FORWARD AGC DESIGN CONSIDERATIONS IN TRANSISTORIZED TELEVISION RECEIVERS*

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I INTRODUCTION

Similar considerations govern the agc circuit design of both tube and transistor television receivers.

The choice of agc delay is a compromise between signal-to-noise ratio at the second detector and overload in the early stages. This requires that either the gain versus agc voltage of each controlled stage should be predictable or that the transistors be supplied in matched kits. The former is of course to be preferred.

II CHARACTERIZING AGC TRANSISTORS

The Fairchild Semiconductor agc transistors are the SE5001 and SE5002 for i-f applications and the SE5003 which is intended for r-f use. These transistors are being fully characterized to provide the designer with pertinent data for both r-f and i-f design. D-c parameters, common-emitter "y" parameters versus temperature at 200 Mc, and agc characteristics at 45 Mc and 200 Mc will be available. The 45-Mc agc characteristics are obtained using the circuit shown in Fig. 1. The gain is measured at a collector current of 4 mA and 22 db minimum power gain is guaranteed. Typical devices give a power gain of 30 db in this test circuit. The agc performance is checked by measuring the increase in collector current required to reduce the gain by 30 db.

Figure 2 shows a graph of transistor agc characteristics obtained by this method. Note that the SE5001 and the SE5002 are biased at 4.0 mA I_C for maximum gain at 9 mA and 11 mA, respectively, for 30 db gain reduction. Knowing these bias conditions the designer can obtain two-point agc tracking.

III AGC I-F AMPLIFIER

A three-transistor i-f amplifier has been constructed for evaluation of the SE5001 and SE5002 transistors. This amplifier has a typical voltage gain of 90 db with an input impedance of 75 ohms and a 5.1 K ohm detector load. The range of agc was measured to be greater than 80 db.

A schematic diagram of the biasing arrangement of the controlled stages of the i-f amplifier is shown in Fig. 3. The control voltage is applied to the base of the second i-f transistor, an SE5001. With the values of resistors shown, 2.9 V from the agc line will bias this transistor to 4 mA emitter current and results in a 1.9 V drop across its 470-ohm emitter resistor. This emitter voltage biases the first i-f transistor, an SE5002, to 4 mA. When the amplifier gain is reduced by 5.7 V of control voltage, the second stage draws 9 mA emitter current. The emitter voltage controlling the first i-f stage increases to 4.2 V and biases the first transistor to 11 mA. Thus the two bias currents specified by the agc characteristic curves for each transistor are obtained and agc tracking results.

An added feature of this agc arrangement is the reduction of the current demanded from the control voltage generator. Using the second stage as an emitter-follower source for the first reduces the current supplied by the control generator to one-half of that required for the shunt-fed system.

Note that the total d-c resistance in the collector-emitter circuit of each i-f stage is approximately 660 ohms. The effect this resistance has on the circuit performance of a typical SE5001 can be seen in Figs. 4, 5, and 6. These graphs were obtained by substituting three values of voltage-dropping resistance in the i-f test circuit previously shown in Fig. 1.

Figure 4 shows that a given reduction in gain can be achieved at lower collector currents by increasing the value of resistance. A limit does exist, however, for the largest value of resistance that will give a usable range of agc. Large resistances decrease the bias current in the emitter-base diode and also decrease the collector-base diode reverse-bias voltage. These two conditions make the transistor susceptible to overload. In the first case overload can result if the i-f signal on the base demands more current than the d-c bias provides. In the latter case, overload can occur if the i-f signal drives the base positive, causing the collector to go negative to an extent where the C-B diode becomes forward-biased. Figure 5 shows the resulting C-B diode reverse-bias voltage when the same three values of circuit resistance are used.

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Even when a 750-ohm resistance was substituted in the test circuit, the reverse-bias voltage remained higher than 5 V at 30 db gain reduction.

With the 660-ohm resistance used in the gain-controlled stages of the three-transistor i-f amplifier, the reverse-bias voltage decreases to a minimum of 3.3 V in the first i-f and 4.6 V in the second i-f under the condition of 80 db gain reduction.

Figure 6 shows another effect resulting from circuit resistance changes. The d-c dissipation in the collector decreases with increasing resistance. Since the maximum dissipation rating of the SE5001 is 500 mW at 25°C and 300 mW at 65°C case temperatures, there is no possibility of over-dissipation with any of the values of resistance shown. The curves also demonstrate the feasibility of using these devices in hybrid sets, where higher ambient temperatures exist.

A schematic diagram of the complete i-f amplifier is shown in Fig. 7. Note that series tuning is used in the base circuits of the controlled stages. Note further that the interstage between the controlled transistors uses a transformer of unity turns ratio. The reason for this design can be explained by examining the "y_{ie}" and "y_{oe}" parameters shown in Fig. 8.

The change in g_{ie} and g_{oe} with increasing current results in the decrease of quantities Q_{ie} and Q_{oe}. If shunt capacitance padding is used, resonant frequency variations can be minimized, but interstage Q cannot be controlled. Series capacitance padding to each controlled base provides a much tighter control of interstage Q and still allows resonant frequency variations to be minimized. Two additional advantages of this technique are: (1) the use of a transformer of unity turns between controlled stages; and (2) the additional gain reduction due to the extreme mismatch conditions under full agc. A complete design and analysis of a television i-f amplifier using this technique are available in Fairchild Application Note APP-71.

Figure 9 shows the gain-control characteristics of the i-f amplifier. Both limit and median SE5001's and SE5002's were evaluated in the 9 possible combinations. The graph shows that if r-f agc is to be delayed by a fixed gain reduction of the i-f amplifier, a potentiometer is required in the resistive divider of the control voltage generator. For a 30 db gain reduction of the i-f before application of agc to the r-f, the control voltage must be adjustable from 4.4 V to 5.6 V. Since the current range for maximum gain is relatively broad in these agc devices, a small error in the current will not appreciably affect the gain. If a fixed voltage of, say, 5 V is selected as the delay level, the i-f amplifier gain reduction will lie between 13 db and 45 db.

The complete i-f amplifier was built on a printed board with dimensions of 2" by 4.5".

It was designed for a video output of 3 V, but the output can increase to 9 V before limiting occurs. Figure 10 shows the output bandshape at three conditions of agc. For these curves, the traps were removed to show uniformity of bandshape. The bandshape is typical for randomly selected units. It was observed that little or no retuning was required with the limit range of transistors and that fixed neutralization could be employed.

IV AGC R-F AMPLIFIERS

The agc transistor for r-f applications is the SE5003. It has a guaranteed minimum 200 Mc power gain of 15 db and a maximum noise figure of 5.5 db. A typical curve of the current-gain bandwidth product versus collector current is shown in Fig. 11.

Agc delay could be introduced simply by biasing the transistor at a collector current which is slightly lower than that for maximum f_t. The noise figure is relatively constant in the range of I_C from 1 mA to 5 mA. There are, however, two disadvantages to using this method: (1) the cross-modulation performance of the device is poorer at lower currents; and (2) the variation of resonant frequency of the input circuit is quite severe.

The reason for the latter disadvantage can be explained with the help of Fig. 12, which shows resistive and reactive components of the h_{ie} versus I_C at four frequencies within the vhf television band. Note that the greatest change in the reactive component of h_{ie} occurs in the range of I_C from 1 mA to 4 mA. Biasing for self-incorporated agc delay will result in operation within this range. If external delay is used with an I_C of 4 mA at the initial condition and with series capacitance padding, the variations in resonant frequency can be minimized.

The cross-modulation characteristic of the SE5003 and the SE3001 are compared in Fig. 13. The SE3001 is a conventional UHF silicon planar device. The interfering signal level represents the voltage applied at the base of the transistor, which must be doubled to represent the voltage at the 300-ohm input. Signal levels shown are of the amplitude that will produce 1% cross modulation. The measurements were taken under the following conditions: no input selectivity; a 1 mV unmodulated desired signal at 200 Mc; and an interfering signal at 150 Mc with 30% 1-Kc modulation.

The gain-control characteristics of the SE5003 at 200 Mc are shown in Fig. 14. Worst-case design of the r-f amplifier should assume that a high current limit SE5003 is used. This ensures that the mixer never overloads.

Therefore, if a voltage-dropping resistance of 500 ohms is employed, the r-f amplifier should be biased at 13 mA I_C for a corresponding i-f amplifier gain reduction of approximately 80 db.

V KEYED AGC DESIGN

The agc circuit shown in Fig. 15 provides the range and r-f delay necessary. The typical i-f amplifier gain-reduction curve previously shown in Fig. 7 was used for this design. The threshold level is the sum of V_{be} and a voltage derived from a divider network in the emitter of the keyer stage. When the input signal exceeds the threshold level during the horizontal sync pulse, the keyer turns ON. The resistive divider in the collector of the inverter stage is selected so that in the maximum gain condition 2.9 V of control is applied to the i-f amplifier.

Diodes D_1 and D_2 are back-biased so that the r-f control voltage is 2.6 V determined by the 7.5 K and 2.2 K resistive divider. Therefore, at maximum gain, all three transistors are biased at approximately 4 mA I_C. When the gain is reduced by 30 db in the i-f amplifier, D_1, D_2, and D_3 become forward-biased. As D_1 and D_2 start to conduct, agc is applied to the r-f amplifier. The conduction of D_3 slows down the i-f amplifier gain reduction by introducing a voltage divider in the i-f agc line. The circuit values are such that when 80 db of i-f gain reduction is achieved, the r-f amplifier collector current is approximately 13 mA. Agc tracking is now established between the i-f and r-f amplifiers.

A complete design and analysis of a keyed automatic gain control circuit using this technique are available in Fairchild Application Note APP-69.

VI CONCLUSION

The signal conditions for optimum agc of a transistor television receiver parallel those which are optimum for tubes. The dissimilarity primarily stems from the techniques used to obtain this performance. Familiarity with transistor terms and operating conditions helps reduce the problems involved to those of basic receiver design. If these differences are understood, transistor sets can be designed with performance comparable to the best tube receivers.

ACKNOWLEDGMENTS

The author expresses his thanks to J. A. MacIntosh for his design suggestions, and M. J. Vellequette for supplying the agc characterization information.

REFERENCES

1. Richard Q. Lane, "I-F Amplifier Design for Transistor TV Receivers," Fairchild Application Note APP-71.

2. Harry S. Suzuki, "VHF Tuner Design for Transistor TV Receivers," Fairchild Application Note APP-72.

3. Samuel A. Schwartz, "Keyed Automatic Gain Control for TV Receivers," Fairchild Application Note APP-69.

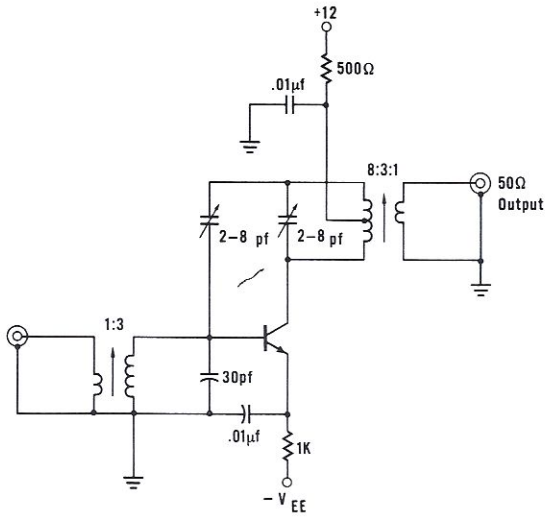


FIG. 1. I-F test circuit.

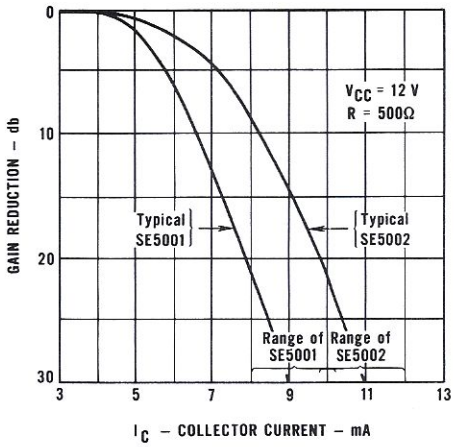


FIG. 2. AGC characteristics of SE5001 and SE5002 at 45 MC/S.

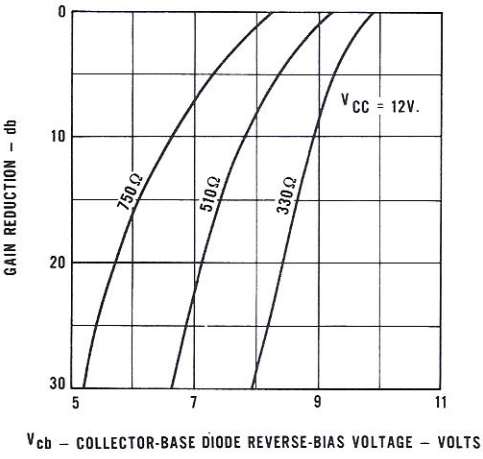


FIG. 5. Gain reduction versus collector-base diode reverse bias voltage of SE5001.

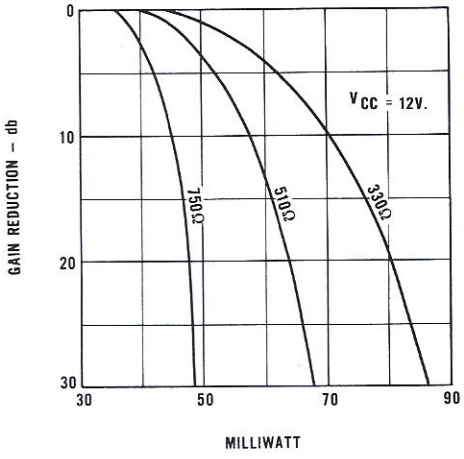
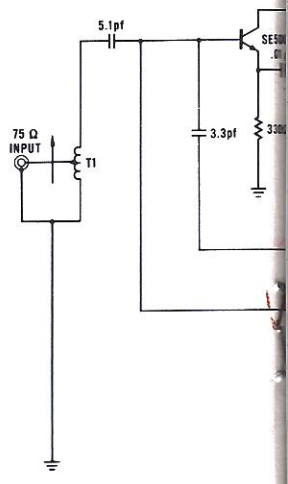


FIG. 6. Gain reduction versus DC collector dissipation of SE5001.

FIG. 7. Schematic diagram



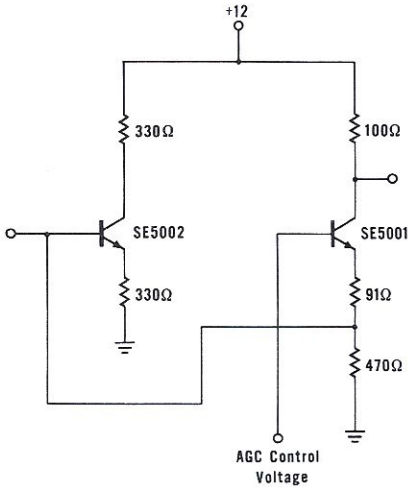


FIG. 3. Biasing arrangement of gain controlled I-F stages.

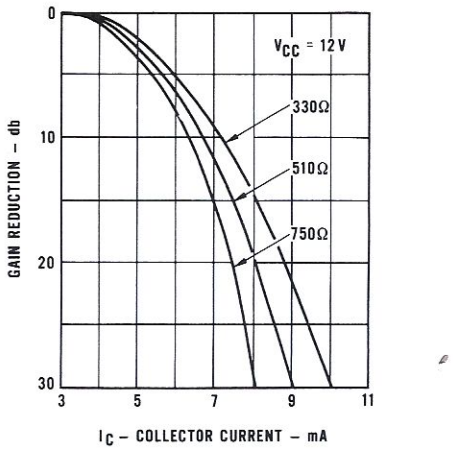


FIG. 4. Effect of voltage dropping resistance on AGC characteristics of SE5001.

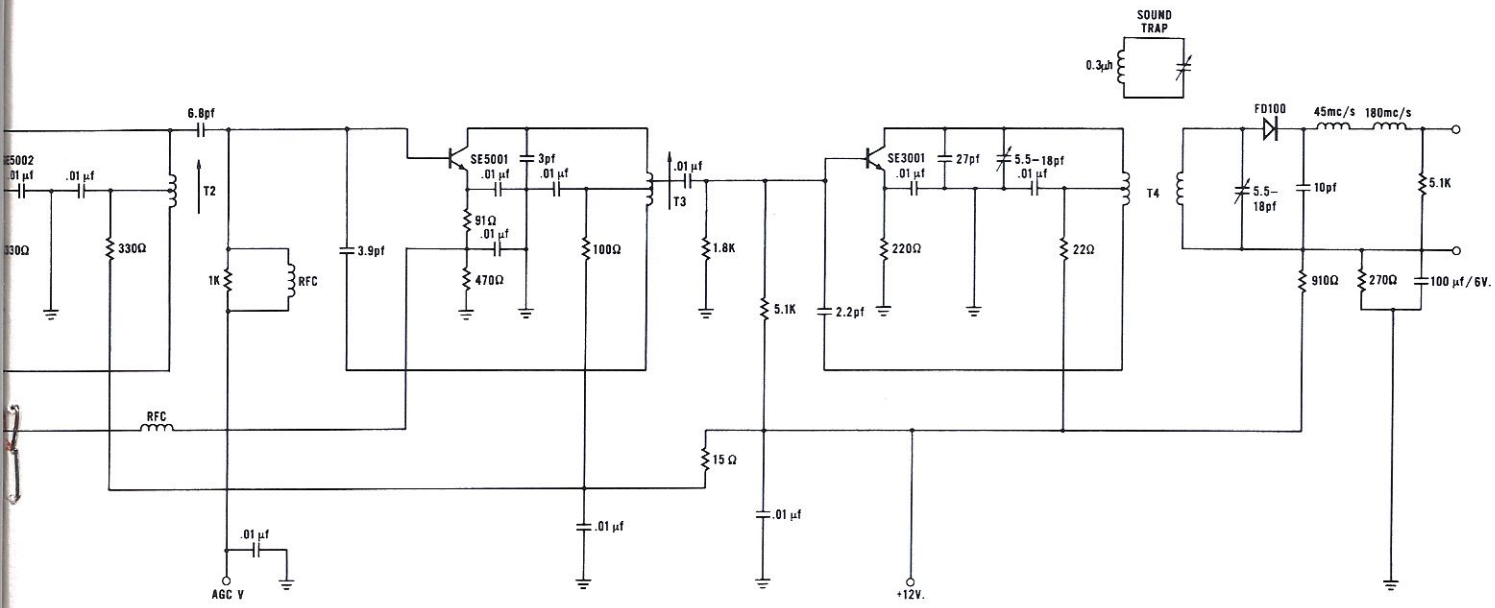
n of 45 MC/S I-F amplifier.

T1 19 turns #36 enameled wire tapped 3 turns from ground wound on micrometals L52-6 shielded coil form

T2 12 turns #36 enameled wire tapped 10:2. Wound on micrometals L-52-6 shielded coil form

T3 14 turns #36 enameled wire tapped 10:2:2. Wound on micrometals L-52-6 shielded coil form

T4 Primary 6 turns #36 enameled wire tapped 4:2. Wound on sickles form #217-5401-1.
Secondary 8 turns #36 enameled wire. Wound on adjustable sleeve.
Sound trap on adjustable sleeve.



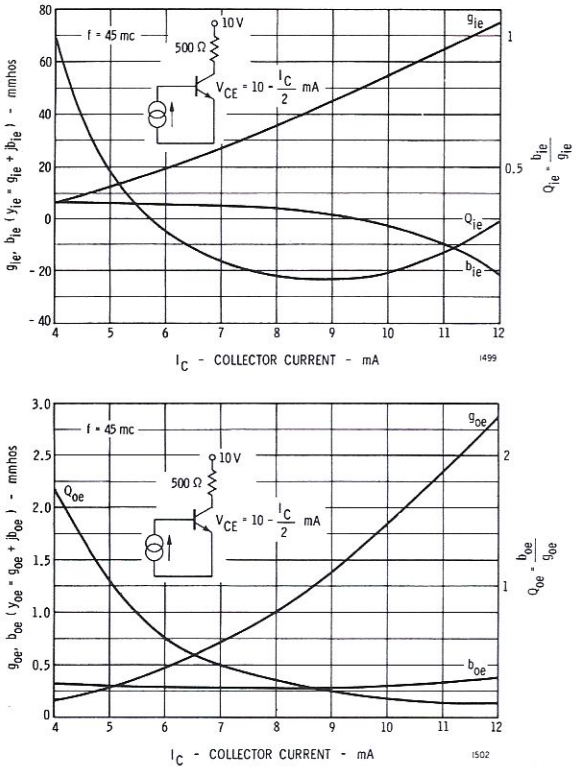


FIG. 8. 45 MC Y_{ie} and Y_{oe} of SE5001 and SE5002.

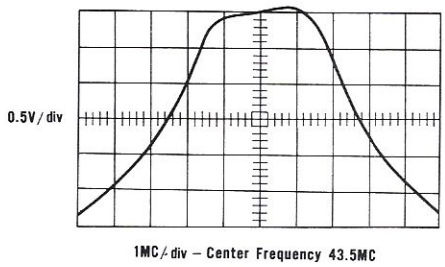


FIG. 10A. Bandshape of I-F amplifier at maximum gain.

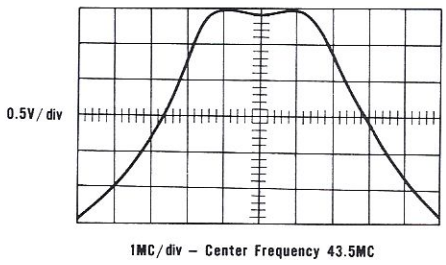


FIG. 10B. Bandshape of I-F amplifier at 30 db gain reduction.

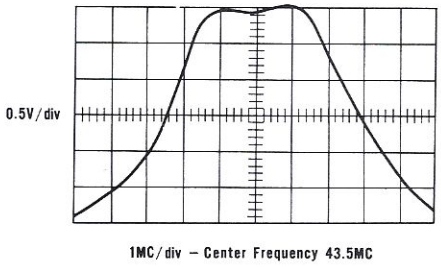


FIG. 10C. Bandshape of I-F amplifier at 60 db gain reduction.

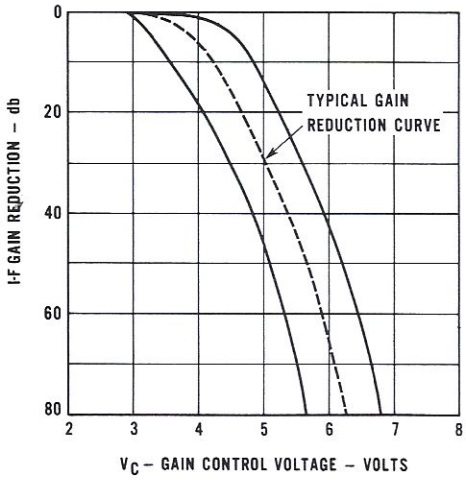


FIG. 9. I-F gain reduction versus AGC control voltage — limit curves.

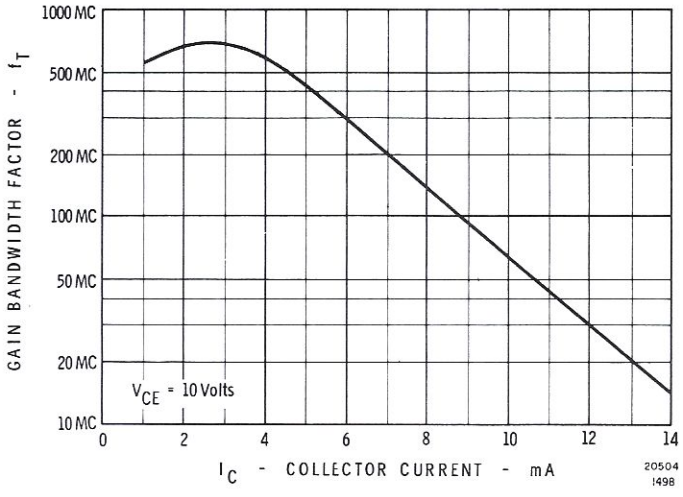


FIG. 11. Current gain bandwidth product versus I_C for SE5003.

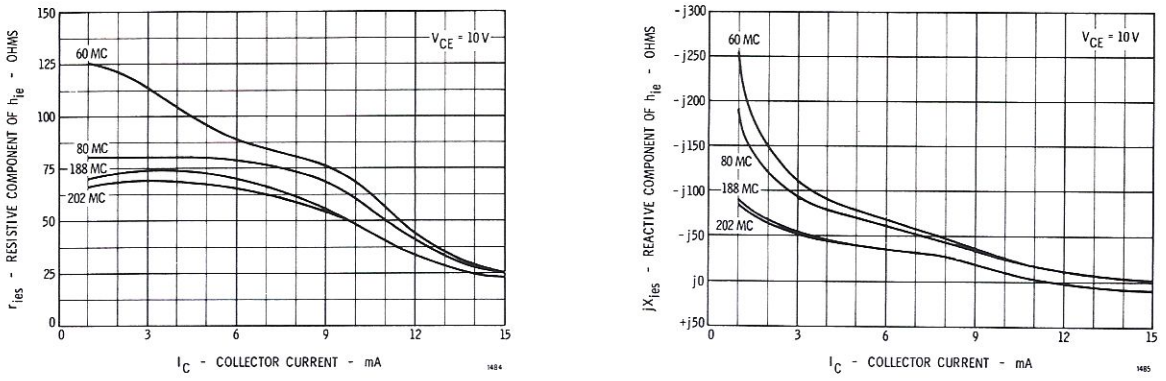


FIG. 12. h_{ie} characteristic of SE5003.

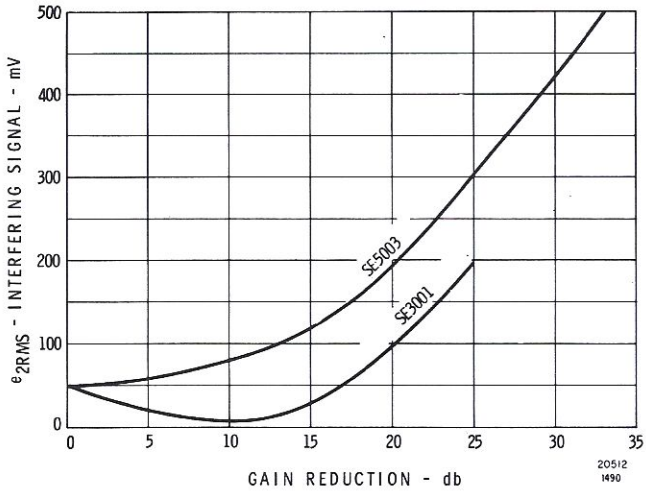


FIG. 13. Cross modulation comparison of SE5003 and SE3001.

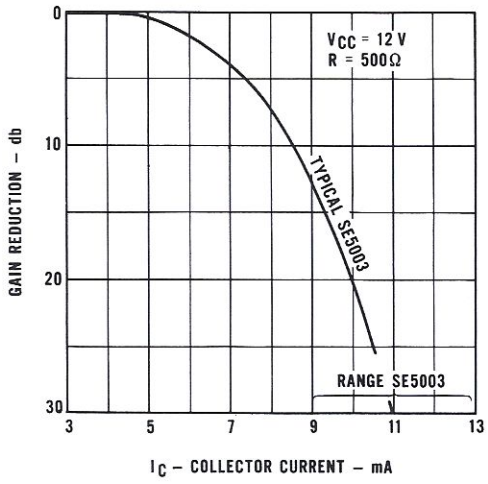


FIG. 14. AGC characteristics of SE5003 at 200 MC/S.

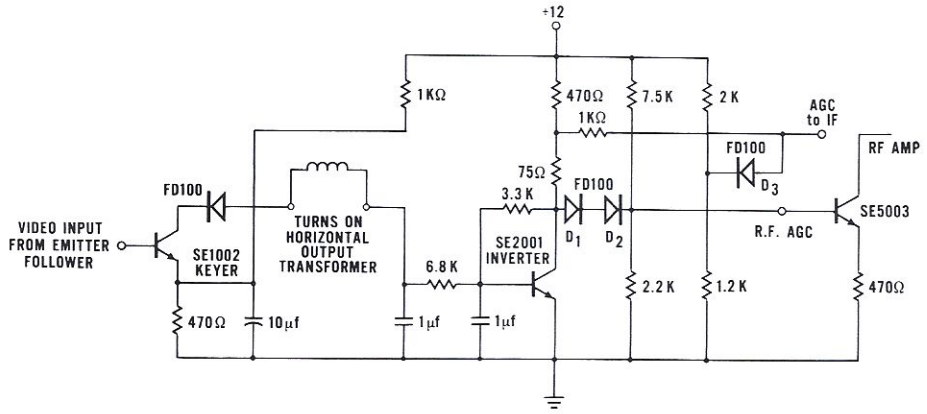


FIG. 15. Schematic of keyed automatic gain control circuit.